REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 13 remain in this case. Claim 2 is amended.

Applicants note the requirement for a new oath or declaration. A newly executed declaration is filed with this paper. Applicants submit that this declaration satisfies the requirements of the Rules of Practice, and overcomes the objection.

The Examiner objected to the drawings, specifically Figure 6, as showing reference numerals that are not referred to in the specification. Amendment to paragraph [30] of the specification is presented to render its description consistent with Figure 6, by changing the reference numerals in the specification. Applicants respectfully submit that this amendment to the specification overcomes the objection to the drawings, without requiring amendment to the drawings.

The specification was objected to as not including the serial number of a related application. The first paragraph on page 1 of the specification is amended above to provide that serial number. No new matter is presented by this amendment. Applicants respectfully submit that this amendment overcomes the objection to the specification, and request its entry.

Claim 2 was rejected under §112, ¶2, as indefinite for failing to particularly point out and distinctly claim the invention. Specifically, the claim was rejected as lacking antecedent basis for the phrase "the identifier value", due to the claim depending upon itself. Claim 2 is amended to depend upon claim 1, consistent with the Examiner's interpretation of the claim. Applicants respectfully submit that amended claim 2 is sufficiently definite to meet the requirements of §112, ¶2.

Claims 1 through 7 and 10 through 12 were rejected under §102(e) as anticipated by the Kakeda et al. reference[1]. Relative to claim 1, the Examiner asserted that the Kakeda et al. reference discloses all of the steps of the claimed method, interpreting the disclosed checking of "global bits" in the Kakeda et al. reference, to determine whether a comparison of a process ID is required, as corresponding to the detecting of an error condition "because the global bits act as error flags".[2] Similarly, relative to independent apparatus claim 11, the Examiner asserted that the Kakeda et al. reference discloses all of the elements of the system, interpreting the disclosed "comparison information storage means" as "abort circuitry", checking global bits to determine whether a comparison of a process ID is required, as corresponding to the detecting of an error condition.[3]

Claims 8 and 9 were rejected under §103 as unpatentable over the Kakeda et al. reference in view of the Gunji reference[4]. The Examiner admitted that the Kakeda et al. reference fails to disclose the memory transaction as being from a direct memory access engine or from a co-processor, but that the Gunji reference discloses a DMA transaction (corresponding also to the co-processor) and would have been obviously combined with the teachings of the Kakeda et al. reference to alleviate the burden on the main processor.[5]

Claim 13 was rejected under §103 as unpatentable over the Kakeda et al. reference in view of the Singh reference[6]. The Examiner admitted that the Kakeda et al. reference fails to disclose the display, RF circuitry, and aerial, but that the Singh teachings regarding a task management system for a handheld computer, which would have been obviously combined with the teachings of the Kakeda et al. reference so that the PDA of the Singh reference could keep track of the tasks without user intervention.[7]

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[1] U.S. Patent No. 6,564,311 B2, issued May 14, 2003 to Kakeda et al.
[2] Office Action of April 16, 2004, page 4, ¶ 10.
[3] Office Action, *supra*, page 7, ¶ 18.
[4] U.S. Patent No. 5,487,154, issued January 23, 1996 to Gunji.
[5] Office Action, *supra*, pp. 8 and 9, ¶¶ 22 and 23.
[6] U.S. Patent No. 6,487,447, issued May 14, 2002 to Singh.
[7] Office Action, *supra*, page 9, ¶25.

Applicants respectfully traverse the rejection of the claims in this case, on the grounds that the teachings of the Kakeda et al. reference fall short of the requirements of the independent claims, and that there is no suggestion from the prior art to modify these teachings in such a manner as to reach the claims.

The method of claim 1 requires the step of detecting of an error condition that prevents normal completion of a memory transaction that was requested responsive to a first one of a plurality of program tasks, and the step of recovering from this error condition by using an identifier value provided with the memory transaction request, to identify that first program task as the source of the memory transaction request. As described in the specification, this method provides important advantages in the operation of a digital system, by enabling the recovery of the system from an error by identifying all entries in a translation lookaside buffer (TLB) that are associated with the task causing an error,[8] and by enabling the rapid killing of a faulty application without impacting others of the plurality of program tasks that are then operating.[9]

Contrary to the assertion by the Examiner, Applicants submit that the Kakeda et al. reference nowhere discloses the detecting and recovering steps required by claim 1 and its dependent claims. Applicants do not disagree with the Examiner that the reference teaches the checking of global bits in entries of a TLB to determine whether a comparison of a process identifier in its TLB entries is required.[10] However, Applicants do disagree with the Examiner's assertion that the global bits act as error flags, and disagree with the Examiner's interpretation of these teachings as corresponding to the detecting of an error condition.[11]

A fair reading of the Kakeda et al. reference, including the locations cited by the reference, leads the reader to understand that each entry of the disclosed TLB includes (along with the virtual and physical page numbers) a process identifier used to effect the address translation, considering that each process can independently set a virtual address space and that

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[8] Specification of S.N. 09/932,378, page 11, ¶ 17.
[9] Specification, *supra*, pp. 16 and 17, ¶ 35.
[10] Office Action, *supra*, page 4, ¶ 10.
[11] Office Action of April 16, 2004, page 4, ¶ 10.

therefore the virtual addresses used by the processes may overlap.[12] The Kakeda et al. reference further discloses that, in some cases, multiple process can share the same virtual address space; in this case, the global bit is set for the TLB entry so that the process identifier in the TLB entry need not match the accessing process.[13] Therefore, from a fair reading of the reference, the global bits do not "act as error flags". Rather, the reference teaches that a TLB entry with a "set" global bit is to effect virtual-to-physical address translation without regard to the process identifier value. There is simply nothing in the Kakeda et al. reference that would lead the skilled artisan to understand that the global bits in its TLB entries are in any way error flags.

Therefore, because the global bits of the Kakeda et al. reference are not error flags, the Examiner is in error in asserting that the checking of the global bits taught by the reference corresponds to detecting an error condition. Instead, the checking of the global bits disclosed by the Kakeda et al. reference merely determines whether the process identifier is to be examined; in either case (global bit set or global bit clear), the TLB of the Kakeda et al. reference goes on to effect the memory access.[14] This operation as disclosed by the Kakeda et al. reference is not the detecting of any error condition, much less the detecting of an error condition that prevents normal completion of the memory transaction (considering that the Kakeda et al. reference continues the memory address translation and access regardless of the value of the global bit).

Accordingly, Applicants respectfully submit that the Kakeda et al. reference fails to disclose the detecting step required by independent method claim 1 and its dependent claims. And as a result, Applicants further submit that the reference necessarily fails to disclose the step of recovering from the error condition by using an identifier value provided with the memory transaction, as is also required by claim 1 and its dependent claims.

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[12] Kakeda et al., *supra*, column 2, lines 13 through 24.
[13] Kakeda et al., *supra*, column 2, lines 43 through 52.
[14] Kakeda et al., *supra*, column 2, lines 53 through 65.

For this reason, Applicants respectfully submit that claim 1 and its dependent claims are all novel over the Kakeda et al. reference. The §102 rejection of claims 1 through 7 and 10 is therefore respectfully traversed.

Applicants further submit that there is no suggestion from the prior art to modify the teachings of the Kakeda et al. reference in such a manner as to reach the requirements of claim 1 and its dependent claims.

First, neither of the other applied references disclose the detecting and recovering steps required by claim 1, nor were they asserted as so disclosing these steps. Indeed, while the Singh reference appears to be directed to a system that is executing multiple tasks,[15] it nowhere mentions any handling of errored or faulty tasks. Applicants therefore submit that the combined teachings of the applied references fall short of the requirements of claim 1.

Secondly, Applicants submit that there is no suggestion from the prior art to modify these teachings in such a manner as to reach claim 1. This lack of suggestion is especially apparent considering that there is no mention in the Kakeda et al. reference of how task or process errors or faults are handled, much less any suggestion that the process identifier in the TLB should be used to assist in the recovering from such an error or fault. Indeed, one can reasonably conclude that the Examiner improperly used Applicants' own teachings, in hindsight, in asserting that the global bits of the Kakeda et al. reference "act as error flags", because there is simply nothing in the reference that suggests this interpretation. And as mentioned above, the Singh and Gunji references provide no teachings relative to the detecting of or recovering from an error in one of a plurality of tasks. Accordingly, the important advantages provided by the invention of claim 1 and its dependent claims, in providing rapid recovery of a system from an error in one application or task without impacting others, stem directly from the differences between the method of claim 1 and the properly combined teachings of the prior art, supporting the patentability of these claims.

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[15] *See* Singh, *supra*, Abstract.

For these reasons, therefore, Applicants both traverse the §102 rejection of claims 1 through 7 and 10 and the §103 rejection of claims 8 and 9, and also respectfully submit that claim 1 and all of its dependent claims are patentably distinct over the prior art of record in this case.

Independent apparatus claim 11 requires, in a digital system having a processor with an address output port, identifier circuitry connected to the processor for holding an identifier value indicative of a program task being executed, and abort circuitry that stores a fault address provided on the address output port and an identifier value corresponding to the fault address in response to a memory transaction error. The claimed apparatus further requires that the processor is operable to read the stored fault address and the stored identifier value. As a result of this construction, the claimed system is capable of recovering from an error in one of a plurality of tasks, by identifying the identifier value of the faulty task,[16] and thus is capable of rapidly killing a faulty application without impacting other program tasks being executed.[17]

Applicants also respectfully traverse the §102 rejection of claims 11 and 12, on the grounds that the Kakeda et al. reference fails to disclose the abort circuitry and processor of the claimed system.

First, Applicants submit that the Examiner is in error in asserting that the Kakeda et al. reference discloses the abort circuitry of claim 11. The rejection is based on the Examiner's finding that the global bits of the TLB in the Kakeda et al. reference "act as error flags".[18] As discussed above relative to claim 1, the global bits of the reference do not "act as error flags" but instead identify, when set in a TLB entry, that the virtual-to-physical memory address translation using that entry can be effected without regard to the process identifier value. The state of the global bit in the TLB entry simply does not indicate, one way or the other, that an error exists. Instead, these global bits simply control how the TLB translation is to be carried

[16] Specification of S.N. 09/932,378, page 11, ¶ 17.
[17] Specification, *supra*, pp. 16 and 17, ¶ 35.
[18] Office Action, *supra*, page 7, ¶18.

out. There is simply nothing in the Kakeda et al. reference that would lead the skilled artisan to understand that the global bits in its TLB entries act as error flags in any way.

Because the global bits of the Kakeda et al. reference are not error flags, the Examiner is in error in asserting that the comparison information storage means of the reference, by its checking of the global bits, corresponds to the abort circuitry of claim 11. As discussed above, the checking of the global bits disclosed by the Kakeda et al. reference merely determines whether the process identifier is to be examined; in any event, the TLB of the Kakeda et al. reference goes on to effect the memory access. There is no circuitry in the Kakeda et al. reference that stores a fault address at the address output port of the processor, or an identifier value corresponding to that fault address, in response to a memory transaction error. Indeed, there is no mention in the Kakeda et al. reference of any circuitry that is responsive to a memory transaction error. Accordingly, Applicants respectfully submit that the Kakeda et al. reference fails to disclose the abort circuitry required by independent apparatus claim 11 and its dependent claims, and necessarily fails to disclose the claim limitation that the processor of the claimed system is operable to read the fault address and identifier value stored by that abort circuitry.

For this reason, Applicants respectfully submit that claims 11 through 13 are all novel over the Kakeda et al. reference. The §102 rejection of claims 11 and 12 is therefore respectfully traversed.

Applicants further submit that there is no suggestion from the prior art to modify the teachings of the Kakeda et al. reference in such a manner as to reach the requirements of claim 11 and its dependent claims 12 and 13.

First, as discussed above relative to claim 1, neither of the other applied references disclose the abort circuitry of claim 11, nor were they asserted as so disclosing that circuitry. The combined teachings of the applied references therefore fall short of the requirements of claim 11.

Secondly, Applicants submit that there is no suggestion from the prior art to modify these teachings in such a manner as to reach claim 11. As discussed above, there is no mention in the Kakeda et al. reference of any circuitry for handling task or process errors or faults, much less suggestion of circuitry that should store a fault address and the task identifier value. The Singh and Gunji references add no teachings regarding these elements. As a result, the advantages provided by the claimed system are the direct result of the differences between the claim and the prior art. Therefore, the lack of suggestion in the prior art of the missing elements of claim 11, and the important advantages provided by the claimed system because of those missing elements, support a finding that claims 11 through 13 are patentably distinct over the prior art.

For these reasons, therefore, Applicants both traverse the §102 rejection of claims 11 and 12 and the §103 rejection of claim 13, and also respectfully submit that claims 11 through 13 are patentably distinct over the prior art of record in this case.

The other references cited by the Examiner but not applied have been considered, but are not felt to come within the scope of the claims in this case.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of the above-referenced application is therefore respectfully requested.

Respectfully submitted,

Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

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Rodney M. Anderson
Registry No. 31,939